WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device having a plurality of memory cells formed on a semiconductor substrate, each made up by electrically connecting a resistor element in series with a field effect transistor;

the resistor element comprising stacked layer films formed of a first electrode layer, a phase change material layer made of one phase change material layer or plural phase change material layers with resistance values changing by heating treatments, and a second electrode layer, deposited in that order, and connected to a power source terminal common to the respective field effect transistors in at least two of the memory cells.

2. A semiconductor integrated circuit device comprising a plurality of memory cells formed on a semiconductor substrate, each made up by electrically connecting a resistor element in series with a field effect transistor;

the field effect transistor having either of a source and a drain, connected to a conductive film serving as bit lines of the memory cells, respectively, and the other of the source and the drain, connected to the resistor element;

the resistor element comprising stacked layer films made up of a first electrode layer, a phase change material layer made of one phase change material layer or plural phase change material layers with resistance values changing by heating treatments, and a second electrode layer, deposited in that order,

and being formed on the conductive film through the intermediary of an insulation film so as to be connected in common to the other of the source and the drain, in at least two of the memory cells.

3. A semiconductor integrated circuit device comprising a plurality of memory cells formed on a semiconductor substrate, each made up by electrically connecting a resistor element in series with a field effect transistor;

the field effect transistor having either of a source and a drain, connected to a conductive film serving as bit lines of the memory cells, respectively, and the other of the source and the drain, connected to the resistor element;

the resistor element comprising stacked layer films made up of a first electrode layer, a phase change material layer made of one phase change material layer or plural phase change material layers with resistance values changing by heating treatments, and a second electrode layer, deposited in that order, and formed on the conductive film through the intermediary of an insulation film so as to be individually connected to the respective field effect transistors in the memory cells.

4. A semiconductor integrated circuit device comprising a plurality of memory cells formed on a semiconductor substrate, each made up by electrically connecting a resistor element in series with a field effect transistor;

the field effect transistor having either of a source

and a drain, connected to a conductive film serving as bit lines of the memory cells, respectively, and the other of the source and the drain, connected to the resistor element;

the resistor element comprising stacked layer films made up of a first electrode layer, a phase change material layer made of one phase change material layer or plural phase change material layers with resistance values changing by heating treatments, and a second electrode layer, deposited in that order, formed on the conductive film through the intermediary of an insulation film and configured such that the first electrode layer and the phase change material layer are divided by the memory cell and the second electrode layer is connected to a power source terminal common to the respective field effect transistors in at least two of the memory cells.

5. A semiconductor integrated circuit device according to claim 1, wherein either of a source and a drain, in the field effect transistor, is connected to the first electrode layer with a plug layer made up by filling up a contact hole, formed in an insulation film, with a conductive material.

6. A semiconductor integrated circuit device according to claim 5, wherein the plug layer comprises a first plug layer connecting the other of the source and the drain, in the field effect transistor, with the bit lines, and

a second plug layer extended on the first plug layer and connected to the first electrode layer.

7. A semiconductor integrated circuit device according to claim 6, wherein the second plug layer is smaller in cross sectional area than the first plug layer.

8. A semiconductor integrated circuit device according to claim 6, wherein the second plug layer has an insulation thin film deposited along an inner peripheral sidewall of the contact hole.

9. A semiconductor integrated circuit device according to claim 6, wherein the second plug layer comprises a first conductive layer having a first resistance value and a second conductive layer having a resistance value higher than the first resistance value, and the second conductive layer is connected to the phase change material layer.

10. A semiconductor integrated circuit device according to claim 1, wherein the phase change material layer comprises stacked layer films formed of a first phase change material layer made of a first melting point material, and a second phase change material layer made of a material having a melting point higher than that of the first melting point material layer, deposited in that order, and

the first phase change material layer is connected to either of the source and the drain, in the field effect transistor.

11. A semiconductor integrated circuit device according to claim 1, wherein the phase change material layer comprises a first phase change material layer in a crystallized state.

12. A semiconductor integrated circuit device according to claim 1, wherein the phase change material layer comprises a second phase change material layer in an amorphous state.

13. A semiconductor integrated circuit device according to claim 1, wherein the phase change material layer comprises stacked layer films formed of a first phase change material layer in a crystallized state, and a second phase change material layer in an amorphous state, deposited in that order, and

the first phase change material layer is connected to either of the source and the drain, in the field effect transistor.

14. A semiconductor integrated circuit device according to claim 1, wherein the phase change material layer comprises stacked layer films formed of a first phase change material layer in an amorphous state, and a second phase change material layer in a crystallized state, deposited in that order, and

the first phase change material layer is connected to either of the source and the drain, in the field effect transistor.

15. A semiconductor integrated circuit device according to claim 1, wherein the phase change material layer comprises stacked layer films formed of a first phase change material layer in an amorphous state, and a second phase change material layer in a crystallized state, deposited in that order, and

the first phase change material layer is connected to either of the source and the drain, in the field effect transistor, with a plug layer formed in a insulation film, having an area

where a portion of the first phase change material layer is crystallized due to Joule heat generated by flow of current to the plug layer.

16. A semiconductor integrated circuit device according to claim 1, wherein any material selected from the group consisting of TiN, TiAlN, and PolySi is provided in a portion of the second plug layer, connected to the resistor element.

17. A semiconductor integrated circuit device according to claim 1, wherein a molybdenum material is provided in a portion of the second plug layer, connected to the resistor element.

18. A semiconductor integrated circuit device comprising a plurality of memory cells formed on a semiconductor substrate, each made up by electrically connecting a resistor element in series with a field effect transistor;

the field effect transistor having either of a source and a drain, connected to the resistor element;

the resistor element comprising stacked layer films made up of a first electrode layer, a phase change material layer made of one phase change material layer or plural phase change material layers with resistance values changing by heating treatments, and a second electrode layer, deposited in that order;

the second electrode layer deposited on the phase change material layer of the stacked layer films, serving as bit lines, and being configured so as to be connected in common to the other of the source and the drain, in at least two of the memory cells.